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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,610	11/28/2001	Kuninori Kawabata	100353-00086	9276

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EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,610	KAWABATA ET AL.	
	Examiner	Art Unit	
	Ly D. Pham	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *7-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Request for Continued Examination (RCE) filed November 29, 2004 has been entered.

2. Applicant's Amendment filed October 27, 2004 has been entered. Claims 1 and 3 have been amended. Claims 7 – 20 have been withdrawn.

3. Claims 1 – 6 are presented for the examination.

Claim Objections

4. Claim 1 is objected to because of the following informalities:

In lines 3 – 4, 'a plurality of operating modes' was amended in the claim but is not supported by the specification. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Hwang et al. (US Pat 5,777,491).

Regarding **claim 1**, Hwang et al. disclose a semiconductor device comprising:

data lines over which data are transferred (inherent in all semiconductor devices);

a drive circuit for driving the data lines in a plurality operating modes (col. 3, lines 23 – 25, circuit family for providing desired logic functions), said plurality of operating modes including a dynamic operating mode in which data lines are precharged prior to transfer of data over said data lines (col. 1, lines 61 – 65, and line 66 – col. 2, line 4, note also that dynamic mode inherently requires precharge operation), and including a static operation mode in which the data lines are not precharged prior to transfer of data over said signal lines (col. 3, lines 29 – 31),

wherein said drive circuit drives the data lines in both said operation modes based on a control signal (col. 8, lines 1 – 2, and col. 1, lines 16 – 23, where the 'control circuits' integrated with memories and the like).

7. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsieh et al. (US Pat 4,878,101).

Regarding **claim 1**, Hsieh et al. disclose a semiconductor device comprising:

data lines over which data are transferred (inherent in all semiconductor devices);

a drive circuit for driving the data lines in a plurality of operating modes (fig. 4, 51), the plurality operating modes including a dynamic operating mode in which data lines are precharged prior to transfer of data over said data lines (col. 6, lines 15 – 17),

and including a static operation mode in which the data lines are not precharged prior to transfer of data over said signal lines (col. 6, lines 20 – 22),

wherein said drive circuit drives the data lines in both operation modes based on a control signal (col. 5, lines 3 – 18, control signal generated in control logic 51).

Regarding **claim 2**, Hsieh et al. further disclose the semiconductor as claimed in claim 1, further comprising a memory cell array to which data lines are connected (fig. 4, cell array 52), data read from the memory cell array being transferred over the data lines (fig. 4, bit lines 56).

8. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuo (US Pat 4,766,473).

Regarding **claim 1**, Kuo disclose a semiconductor device comprising:

data lines over which data are transferred (inherent in all semiconductor devices);

a drive circuit for driving the data lines in a plurality operating modes (fig. 5, 51), the plurality operating modes including a dynamic operating mode in which data lines are precharged prior to transfer of data over said data lines (col. 5, lines 60 – 62), and including a static operation mode in which the data lines are not precharged prior to transfer of data over said signal lines (col. 5, lines 66 – 68),

wherein said drive circuit drives the data lines in both operation modes based on a control signal (col. 4, lines 53 – 68, '...appropriate to the operation specified by the control signals applied to logic 51.').

Regarding **claim 2**, Kuo further discloses the semiconductor as claimed in claim 1, further comprising a memory cell array to which data lines are connected (fig. 5, cell array 52), data read from the memory cell array being transferred over the data lines (fig. 5, bit lines 55).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh et al. (US Pat 4,878,101) in view of Furutani et al. (US Pat 5,305,261).

Regarding **claim 3**, Hsieh et al. disclose the semiconductor device as claimed in claim 1, except further comprising the additional limitations as claimed in claim 3. However, Furutani et al. have shown the test dedicated line (col. 5, lines 10 – 12),

wherein a predetermined test of the semiconductor device is performed using the test-dedicated line and the signal lines (fig. 10, test data input 922 connect to signal lines).

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to combine the features shown by Furutani et al. to the disclosure by Hsieh et al., to ensure error-free operation.

Regarding **claim 4**, Furutani further discloses a circuit receiving the signal lines at inputs thereof and outputting a test result (fig. 10, line test circuit 5 outputs test result, shown error in figure), said test result and a logic level of the test-dedicated line forming a result of the predetermined test (dedicated test data line being wired-ANDed implies that its test output has to be a certain logical state).

Regarding **claim 5**, Furutani further discloses a precharge circuit precharging the signal

lines and the test-dedicated line (abstract: the semiconductor memory device further includes a load circuit which precharges the internal data transmitting lines to a predetermined potential in a test mode, and a line test circuit which determines existence and nonexistence of a defective memory cell based on the potentials of the internal data transmitting lines).

11. Claims 3 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuo (US Pat 4,878,101) in view of Furutani et al. (US Pat 5,305,261).

Regarding **claim 3**, Kuo discloses the semiconductor device as claimed in claim 1, except further comprising the additional limitations as claimed in claim 3. However, Kuo has shown the test dedicated line (col. 5, lines 10 – 12),

wherein a predetermined test of the semiconductor device is performed using the test-dedicated line and the signal lines (fig. 10, test data input 922 connect to signal lines).

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to combine the features shown by Furutani et al. to the disclosure by Kuo, so that error-free memory operation is achieved.

Regarding **claim 4**, Furutani further discloses a circuit receiving the signal lines at inputs thereof and outputting a test result (fig. 10, line test circuit 5 outputs test result, shown error in figure), said test result and a logic level of the test-dedicated line forming a result of the predetermined test (dedicated test data line being wired-ANDed implies that its test output has to be a certain logical state).

Regarding **claim 5**, Furutani further discloses a precharge circuit precharging the signal

lines and the test-dedicated line (abstract: the semiconductor memory device further includes a load circuit which precharges the internal data transmitting lines to a predetermined potential in a test mode, and a line test circuit which determines existence and nonexistence of a defective memory cell based on the potentials of the internal data transmitting lines).

12. Claims 2 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang et al. (US Pat 4,878,101) in view of Furutani et al. (US Pat 5,305,261).

Regarding **claim 2**, although Hwang et al. did not clearly show the semiconductor device as claimed in claim 1, further comprising a memroy cell array to which data liens are connected, data read from the memory cell array being transferred over data lines. However, such feature has been shown by Furutani et al. (fig. 1, memory cell array 3) to which the signal lines are connected (signal lines IO in fig. 10), data read from the memory cell array being transferred over the signal lines (fig. 10, test data input 922 transferred over the signal lines).

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to combine the feature shown by Furutani et al., to the circuit shown by Hwang et al., so that memory system with flexible operational mode capabilities is achieved.

Regarding **claim 3**, Hsieh et al. disclose the semiconductor device as claimed in claim 1, except further comprising the additional limitations as claimed in claim 3. However, Furutani et al. have shown the test dedicated line (col. 5, lines 10 – 12), a predetermined test of the semiconductor device being performed using the test-dedicated line and the signal lines (fig. 10, test data input 922 connect to signal lines).

Regarding **claim 4**, Furutani further discloses a circuit receiving the signal lines at inputs thereof and outputting a test result (fig. 10, line test circuit 5 outputs test result, shown error in figure), said test result and a logic level of the test-dedicated line forming

a result of the predetermined test (dedicated test data line being wired-ANDed implies that its test output has to be a certain logical state).

Regarding **claim 5**, Furutani further discloses a precharge circuit precharging the signal

lines and the test-dedicated line (abstract: the semiconductor memory device further includes a load circuit which precharges the internal data transmitting lines to a predetermined potential in a test mode, and a line test circuit which determines existence and nonexistence of a defective memory cell based on the potentials of the internal data transmitting lines).

Allowable Subject Matter

13. **Claim 6** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

14. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly Pham
February 14, 2005

HOAI HO
PRIMARY EXAMINER